GX3700e

MARVIN TEST SOLUTIONS

FPGA PXIE HIGH-PERFORMANCE DIGITAL I/O CARD

- User configurable, on-board Altera Stratix III FPGA
- No proprietary FPGA design tools required
- 160 digital I/O signals available for user specific applications
- x4 PXI Express interface & integral DMA controller supports data streaming rates of more than 800 MB/s
- 700 MHz digital I/O clock rate
- Supports user defined expansion boards for custom interfaces

DESCRIPTION

The GX3700e is a user configurable, FPGA–based, 3U PXI Express card offering 160 digital I/O signals which can be configured for single-ended or differential interfaces. The card employs the Altera Stratix III FPGA, which can support SerDes data rates up to 1.2 Gb/s, digital I/O clock rates of 700 MHz, and features 47,500 logic elements and 2.1 kb of memory. The GX3700e is supplied with an integral expansion board providing access to the FPGA's 160 I/Os. Alternatively, users can design their own custom expansion cards for specific applications - eliminating the need for additional external boards which are cumbersome and physically difficult to integrate into a test system. The design of the FPGA is done by using Altera's free Quartus II Web Edition tool set. Once the user has compiled the FPGA design, the configuration file can be loaded directly into the FPGA or via an on-board EEPROM.

FEATURES

The GX3700e's digital I/O signals are 5 V tolerant. Logic families supported by the I/O interface include LVTTL, LVDS and LVCMOS. The FPGA device supports up to four phase lock loops for clock synthesis, clock generation and for support of the I/O interface. An on-board 80 MHz oscillator is available for use with the FGPA device or alternatively, the PXI 10 MHz or 100 MHz clock can be used as a clock reference by the FPGA.

The FPGA has access to all of the PXI Express bus resources including the PXI 10 MHz clock, PXIe 100 MHz clock, PXIe Sync100, PXIe DStar triggers, the local bus, and the PXI triggers; allowing the user to create a custom instrument which incorporates all of the PXI Express bus resources. The GX3700e includes a DMA controller - facillitating high speed data streaming to and from the host controller.

Control and access to the FPGA is provided via the GX3700e's driver which includes DMA and interrupt support, tools for downloading the compiled FPGA code, and register read and write functionality.

PROGRAMMING AND SOFTWARE

The board is supplied with the GXFPGA library, a software package that includes a virtual instrument panel, and a Windows 32/64-bit DLL driver library and documentation. The virtual panel can be used to interactively program and control the instrument from a window that displays the instrument's current settings and status. In addition, interface files are provided to support access to programming tools and languages such as ATEasy, LabView, LabView/Real-Time, C/C++, Microsoft Visual Basic®, Delphi, and Pascal. An On-Line help file and PDF User's Guide provides documentation that includes instructions for installing, using and programming the board.
A separate software package - GtLinux - provides support for Linux 32/64 operating systems.

APPLICATIONS

- Automatic Test Equipment (ATE)
- Semiconductor test
- Custom interface emulation
- Custom instrumentation
- SerDes interfaces

FPGA

GX3700e

SPECIFICATIONS

EXTERNAL DIGITAL I/O CHANNELS	
Logic Families	LVTTL, LVDS, configurable for 1.2 / 2.5 / 3.3 V logic; 5 V compatible
Output Current	±4.0 mA
Input Leakage Current	±10 µA
Power on State	Default is disconnect at power on (unprogrammed FPGA) or defined by FPGA program
Number of Channels (External Interface)	160 I/O signals, single ended, direction is configurable on a per channel basis Up to 64 I/O can be differential (32 differential channels) (4) I/O are single-ended or (2) differential clock inputs
Protection	Overvoltage: -0.5 V to 7.0 V (input) Short circuit: up to 8 outputs may be shorted at a time
I/O Connector	(4) SCSI III, VHDCI type, 68 pin female
EXPANSION BOARD INTERFACE	
Board ID	4 bits
Digital I/O Interface	160 I/O, signals, single ended, direction is configurable on a per channel basis Up to 64 I/O can be differential (32 differential channels) (4) I/O are single-ended or (2) differential clock inputs
Master Clear	From PXIe interface
Power	±12 V, +5 V, +3.3 V, +2.5 V, +1.2 V
TIMING SOURCES	
PXIe Bus	10 MHz, 100 MHz
Internal	80 MHz oscillator, ±20 ppm
FPGA AND MEMORY	
FPGA Type	Altera Stratix III, EP3SL50F780
Number of PLLs	Four
Logic Elements	47.5 k
Internal Memory	2.133 kb
On-Board Memory	256 k x 32 SSRAM
On-Board Flash	16 MB

POWER	
3.3 VDC	3.6 A (typ); 4.9 A (max)
5 VDC	0.035 A (typ); 0.04 A (max)
12 VDC (For Expansion Board)	Expansion board dependent
ENVIRONMENTAL	
Operating Temperature	0 °C to +50 °C
Storage Temperature	-20 °C to +70 °C
Size	3U PXI
Weight	200 g

Note: Specifications are subject to change without notice

ORDERING INFORMATION

GX3700e	3U PXIe High-Performance FPGA Board
ACCESSORY	
GT95021	2 ft. Shielded Cable for all 5xxx/35xx (68 Pin)
GT95022	3 ft Shielded Cable for all 5xxx/35xx (68 Pin)
GT95028	10 ft shielded cable for 5xxx/35xx products (68 Pin)
GT95031	6 ft Shielded Cable for all 5xxx/35xx (68 Pin)
GX3701	Flex I/O Feed Through Expansion Board for GX3700 / GX3700e FPGA Module
GT95021R	2 ft Shielded Cable for all 5xxx/35xx (68 Pin), reversed back shell on one end
GT95032	1 ft. Shielded cable with 68 Pin SCSI connectors

FPGA