Implementing a High Performance Digital Sub-System Using the PXI Architecture

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Abstract—High performance digital subsystems have been developed over the years using a variety of proprietary and industry standard architectures such as GPIB and VXI. With the availability of high performance / high density FPGAs and analog electronics, the implementation of high performance digital functional test subsystems has now become a reality using the PXI architecture. The smaller form factor of PXI, which offers users the ability to down size and deploy very cost effective, performance digital subsystems, has also presented some unique challenges for instrument design teams developing these high performance digital subsystems.

This paper discusses some major considerations and challenges when implementing high performance digital instrumentation based on the PXI architecture.

Keywords — digital test, PXI digital subystem, depot test, intermediate level test

I. BACKGROUND

The first digital functional test systems were introduced in the late 1960s. In August of 1969, GenRad (General Radio at the time) introduced the GR1790 at the Westcon show. Based on a proprietary architecture and controlled by a PDP-8 computer, the 1790 included 4K of core program memory. Following the introduction of the GR1790, subsequent versions of the 1790 and other competing proprietary digital functional systems were introduced in the 1970s and early 1980s. Systems such as the Teradyne L125, L200 and L300 and the GenRad GR179x and GR2750 were all based on proprietary architectures and relied upon custom digital and analog devices to achieve their digital performance specifications. These systems also shared the characteristics of requiring significant floor space, many kilowatts of input power, and of course a high price tag. Sales prices for these systems could easily exceed $1M USD. Figure 1 shows an example of an early digital functional test system.

In the 1980’s GPIB based digital subsystems were introduced which for the first time, allowed users to integrate and control a digital subsystem as part of a custom test system designed by the end user. While offering the flexibility to integrate a digital subsystem as part of an overall test system and being lower in cost, these types of systems had less pins than proprietary digital functional test systems. In the late 1980s, the emergence of the PC and VXI card modular standards enabled the creation of a new generation of digital instruments - ranging from simple digital instruments implemented on ISA cards to higher performance subsystems implemented using the VXI architecture. The adoption of the card modular architecture was widely accepted by the mid – 1980s for implementing digital subsystems. One of the first VXI digital subsystems was the GenRad AccuWave (Figure 2). Introduced in 1993 and featuring a vector rate of 20 MHz, with 256 low voltage and 64 high voltage channels, and 16 time sets with 1ns timing resolution, the AccuWave represented a new level of performance in card modular digital instrumentation. Subsequent to this system, several other VXI based digital test systems were developed – notably the Teradyne M900, M9, and Talon SR192. With the more compact size associated with VXI-based digital test systems and higher channel counts compared to a GPIB based solution, VXI came to be the dominant architecture for digital subsystems by the late 1990s. However, the need to supply specialized voltages and high power to these systems still required some adaptation of the standard – resulting in the requirement for specialized VXI chassis’s that could support the power and cooling requirements for the pin electronics.

In 1997 the PXI standard was released and shortly after the PXI System Alliance was formed. The first generation of PXI digital instruments was available in the early 2000s and offered cost effective digital test solutions for many digital test applications. However, the ability to offer a PXI based solution with the performance and features associated with high-end VXI digital instruments has only recently been addressed. With the increasing availability of high performance / high density FPGAs and highly integrated analog electronics, high performance digital functional test subsystems based on the PXI architecture are now a reality. By leveraging these various technologies, the compact form factor of PXI now offers users the ability to down size and
deploy very cost effective, performance digital subsystems. The following sections detail how these performance requirements and challenges associated with designing a PXI digital subsystem have been successfully addressed.

II. CONSIDERATIONS

There are several design considerations and challenges one must consider when implementing high performance digital instrumentation based on the PXI architecture. Key factors include:

- Analog or pin electronics – Achieving the best driver / sensor performance and features with high channel count density is always challenging for the instrument designer. For high voltage pin electronics applications, additional consideration must be given to how best to supply the high voltages to these components since the PXI standard offers only limited power and voltages to each PXI slot.

- Managing power requirements and power dissipation – High performance pin electronics require creative and novel ways to manage the power consumption and dissipation for a PXI-based digital instrument. For moderate to high channel count systems, attention must be given to the overall design of the system’s cooling and the chassis design to ensure adequate thermal management of all boards in the system.

- Interface considerations – Providing a high performance interface between the instrumentation and the UUT has historically been a weak point for digital subsystems. With the availability of higher performance connectors, new methods for connecting to the UUT which helps preserve overall signal integrity can be achieved.

- Multiple module synchronization – Digital subsystems are typically comprised of more than one board. A method of controlling all boards in the system or a domain requires that the architecture be able to support inter-board synchronization using the PXI backplane’s signaling resources. A variety functions must be controlled synchronously such as sequencing, branching, conditionals, stop on fail, etc. Additionally, the newest generation of digital subsystems allows multiple instruments to operate independently – requiring that each digital board contain its own sequencer and timing generator as well as vector memory and pin electronics.

III. PIN ELECTRONICS

Historically, pin electronics for digital subsystems have relied upon custom designs – some discrete, some hybrid and some full custom. However, over the past 5 years, a variety of commercial vendors have started producing a range of pin electronic products for both semiconductor and board level test applications. Today, the features and channel densities far exceed what has been done in the past with custom designs and for most applications, the use of commercial devices can accommodate the functional test needs for most markets.

There is always a tradeoff between channel density and pin electronics features. Features such as programmability per pin that supports control of output voltage levels and input threshold levels, slew rate, and parametric measurement capability, require more board space than a simple I/O pin with programmability for groups of eight or more. In addition, these per pin features will require more power and dissipate more heat. Ultimately, the decision regarding pin electronic features rests with how well the proposed design addresses the targeted market. In addition, since PXI products can be implemented in a 3U or 6U form factor, the advantages associated with the larger real estate format need to be weighed against the marketability of a 3U product. For example, the real estate needed to create on-board power supplies for a 3U implementation can significantly impact the number of channels that can be implemented on a 3U versus 6U design.

For addressing legacy mil-aero digital applications, the need for per pin programmability and flexibility becomes a dominant factor for this market segment compared to the PXI form factor. By adopting the 6U form factor and employing highly integrated pin electronics (with all reference levels generated on board and featuring a high level of integration), it is possible to achieve designs with high channel counts without sacrificing features or performance. For example a current PXI design which employs dual channel pin electronics, has been developed that offers 32 digital channels with per pin programmability and an integral sequencer and timing generator.
IV. Power Supplies

According to the PXI specifications, the minimum power that the chassis should provide is 2A for the 3.3V and 5V rails, 0.5A for the 12V rail and 0.25V for the -12V rail. The slot connector pin is limited to 1A, so the maximum current for a PXI card is limited by the number of pins for a rail; 10A for the 3.3V rail, 8A for the 5V rail and 1A for the 12V and the -12V rails. It should be noted that there are few PXI chassis in the marketplace that can supply this maximum current to more than three or four slots so for a high channel count system, it is important to choose a chassis with adequate DC power.

Pin electronics usually require two voltage rails, VH (or VCC) and VL (or VEE), to support the programmable input and output voltage levels. A PXI chassis’s power supply can support low voltage drive /sense levels (-2 to +7V) via an onboard power supply, but for high voltage levels (-10 to +15V) there is not enough PXI system power to generate the required VCC and VEE voltages on board. In this case an off board power supply is needed. To satisfy this requirement, a special power supply mounted in the PXI chassis may be employed or alternatively, an external power supply can be used with VCC and VEE power routed via an additional connector located on the module.

The PXI standard allows for 6U chassis and modules to use the J5/P5 connector for application specific functions. This becomes very useful when the power supply for the pin electronics is mounted in the chassis. In this case the J5/P5 connector can be used for distributing the power to the modules and for controlling the power supply from the digital card. Figure 3a and Figure 3b details several examples of performance PXI digital cards and chassis.

V. Power Dissipation

Fast pin electronics with large voltage swings dissipate a lot of heat. To keep the pin electronics from overheating, a good solid heat sink is required along with ample air flow. Extra fans may also need to be installed in the chassis. Other than this traditional practice, there are other techniques to deal with power dissipation.

One of the ways to manage the power dissipation is to use programmable power supplies for VL and VH and tightly control them by software, based on an application’s specific drive / sense levels. The quiescent power dissipation for the pin electronics is VL+VH times the quiescent current. The actual output’s programmable levels Voh and Vol for a specific application may not be close to the VH and VL rails; however the quiescent power dissipation will still be high regardless of the programmed Voh and Vol levels. Consider the case where the programmable output level range is -10V to +15V. The VH voltage needs to be around 20V and the VL voltage needs to be around -15V to provide head room for the pin electronics circuits. If an application requires Voh=5V and Vol=0V, VH can be programmed down to 10V and VL to -5V. In this case, the pin electronics’ power dissipation will be reduced by more than 50%. By actively managing the VH and VL power supply voltages, power dissipation can be minimized resulting in lower operating temperatures and increased reliability.

Another method to help manage power dissipation is via a programmable slew rate and bias current function. Devices that support this functionality can help minimize power dissipation for those applications that do not require high slew rates or high vector rates.

VI. Interface

An important factor in a digital subsystem’s performance is the interface to the Unit Under Test (UUT). Signal integrity should not be compromised when interfacing high performance digital signals with fast edge rates to the UUT. Controlling the impedance of the traces on the PCB and matching trace lengths will ensure good performance and low channel to channel skew at the module’s connector. Maintaining a high performance transmission path from the instrument to the UUT requires that the connector-cable set offer dedicated signal return lines for each signal and have a characteristic impedance that matches the driver’s source impedance. Additional attributes to consider for the interface connector are a small footprint and a positive, secured mating mechanism. A good example is the VHDCI or SCIS3 connector which readily accommodates off the shelf cable assemblies and offers impedance controlled, twisted pair cabling structure. This type of connector occupies minimal board space and includes a positive mating connection via jack screws.
VII. SYNCHRONIZING MULTIPLE MODULES

Many applications require more digital channels than one module can provide. In this case several modules need to be linked together to form a domain. All modules within a single domain will use the same timing sets allowing all channels to run synchronously. The PXI standard has provisions for interconnecting modules using the trigger bus and local bus. The trigger bus is an eight signal bus that physically connects all slots in one segment (usually six or seven slots) and logically to other segments. The local bus is a twelve signal bus that connects each slot to the adjacent one. For each slot there is one local bus to the left and one to the right except for slot two and the last slot that have only one local bus. Both of these buses can be used for connecting timing signals between the modules. However, the local bus is usually a better choice since it’s not bound by segment size and the interconnecting lines have shorter stubs, offering a higher performance transmission path for timing signals.

VIII. SUMMARY

For almost 40 years, high performance digital subsystems have been available in market place, beginning with proprietary architectures and progressively moving to standards based architectures using the GPIB and VXI architectures. With the availability of high performance / high density FPGAs and analog electronics, the implementation of high performance digital functional test subsystems has now become a reality using the PXI architecture. The flexibility and compact size of the PXI platform now offers users for the first time, a cost effective, high performance, and small footprint digital test solutions which have wide applicability for factory, depot, and field applications.

REFERENCES

[1] PXI Hardware Specification, Revision 2.2, September 22, 2004; PXI Systems Alliance