An FPGA–Based Solution for Testing Legacy Video Displays

Dale Johnson
Geotest – Marvin Test Systems
1770 Kettering
Irvine, CA 92692 USA

Abstract—The theme for Autotestcon 2010 is "45 Years of Support Innovation – Moving Forward at the Speed of Light." This theme is particularly relevant for military ATE systems because it highlights the dichotomy of striving to maintain state-of-the-art testing capabilities, while at the same time needing to support legacy technologies that may be decades old – indeed, as old as Autotestcon itself. The need to support discrete transistor-based electronics, TTL, CMOS and other technologies developed in the 1960's and 1970's, using test systems built around custom ASIC's, high performance FPGA's and logic levels whose peak-to-peak amplitudes were once considered "noise", presents unique challenges.

Systems deployed in the last century used CRT monitors to display information to a technician or operator. These monitors were based on analog video transmission standards such RS170, NTSC (National Television Standards Council), PAL (Phase Alternating Line) and other similar standards. Today, with the widespread use of DVI and HDMI digital video, it is rare to find CRT monitors in commercial use. But they are still widely used in older deployed systems.

This paper is a case study based on the requirement for a PXI-based instrument that can generate simple color bar signals in NTSC and PAL formats to support the Mini-Samson/Katlanit Remote Controlled Weapon Station. By integrating an off-the-shelf PXI FPGA card, with an intellectual property (IP) core available in the public domain and a handful of commercially available support components, a cost effective solution was developed which supports the generation of both analog and digital video signals for testing CRT and LCD monitors. The flexibility of this approach allowed the extension of the original requirement for generating color bar patterns to include more complex test patterns.

Keywords – video generator, PXI video generator, FPGA

I. OVERVIEW

Rafael Systems Division developed the Samson Remote Controlled Weapon Station (RCWS) in the late 1990's [1]. It is a weapon platform that enables a variety of devices to be operated automatically or by remote control. Weapons supported include 5.56 mm, 7.62 mm, and 12.7 mm machine guns, 40 mm automatic grenade launchers, anti-tank missiles and observation pods. A variation of the Samson RCWS, called Mini-Samson, or Katlanit, was developed in the early 2000's, and first deployed in 2006.

Geotest - Marvin Test Systems was selected to build a system to test components of the Katlanit RCWS. The TS-230 test system was designed to comprehensively functionally test the CU (Control Unit), DU (Display Unit) and GCHU (Gun Control Hand Unit) LRU components of the Katlanit weapons system. These integral components comprise 80 percent of the RCWS platform. The CU is the computer of the RCWS system whose functions include monitoring the position of the gun in relation to the vehicle on which it is mounted, providing lock out points inhibiting firing operations based on the vehicle type (i.e., the vehicle gun cannot be fired when within defined parameters relative to the proximity of hatches, or for specified angular relationships to the front of the vehicle), as well as supporting all other RCWS control functions and drive commands. The DU is the control and display unit for the Day and Night sights on the RCWS and displays all image date from these units. The GCHU is the joystick control providing inputs to the CU based on control movement and firing operations initiated by the operator.

The original test requirements for the DU called for a manual test using a custom DU interface test box. The manual-only design made integration more complex, and only allowed for limited system interaction. Future systems will require a Color Bar generator for producing standard NTSC or PAL video signals for automated DU testing. The proposed upgrade to the TS-230 test system includes a PXI-based color bar generator for creating standard NTSC or PAL color bar video signals as well as supporting other patterns that will enhance the ability to measure the display pattern sharpness, black level saturation, viewing angle, and contrast ratio. By developing a PXI version of the color bar generator, the DU interface test box will be eliminated and the PXI replacement will support full automation of the entire test capability for the DU, improving test capabilities, removing unnecessary manual operator intervention during testing and reducing overall test times.

II. IMPLEMENTATION

The proposed solution integrates multiple Commercial Off-The-Shelf (COTS) components with control software to provide a flexible, yet cost-effective solution for testing older NTSC and PAL displays as well as testing VGA monitors. The architecture's core platform is based on the Geotest GX3500, a user configurable 3U FPGA PXI card incorporating the Altera Cyclone III FPGA (Figure 1). Besides the high-performance and gate density of the Altera Cyclone III FPGA, the GX3500 is an ideal platform for this type of application because it can accept an internal mezzanine expansion card assembly that can be used to customize the interface to the UUT, or integrate additional functionality
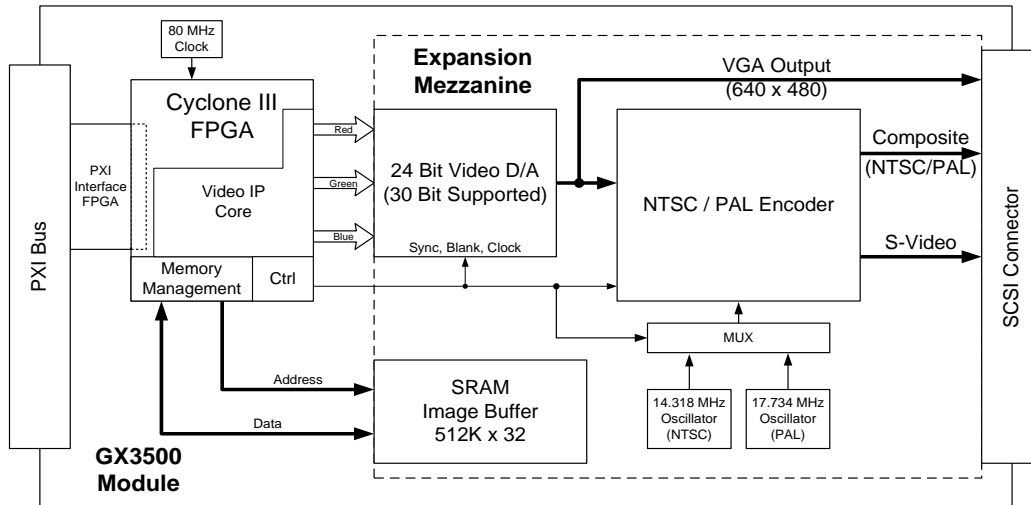
Figure 1 - GX3500-Based Video Pattern Generator Architecture

within the single 3U module. Both capabilities were used in this design.

A. GX3500 FPGA Board

While the capabilities of the GX3500 are varied and robust, a review of its capabilities is beyond the scope of this paper. The GX3500 brings to this application a ready-made PXI platform that hosts the hardware and firmware components for the video generator. The GX3500 has two FPGA's on board. One is dedicated to interfacing to the PXI bus, providing all of the handshaking, address decoding and other overhead functions required of a PXI instrument.

The second FPGA, the Cyclone III, is reserved almost entirely for the user's application. A small section of the Cyclone III hosts some logic to interface to the PXI FPGA. By placing the PXI logic external to the Cyclone III, it is not necessary to integrate a PCI IP core inside the Cyclone, which reduces design integration time and frees up more gates for the application logic – in this case, a video generator. Logic designs for the GX3500's Cyclone III FPGA can be generated using Altera's Quartus II Web Edition Software development toolset, available for free from the Altera web site [2].

B. Video Generator IP Core

The heart of the video generator is a VGA Controller IP core provided by Altera in an open-source format [3]. As the original intent of the project was to produce NTSC and PAL composite video, a VGA IP was selected as it produces resolutions similar to these standards. The VGA Controller generates the video data with vertical and horizontal synchronization timing and provides the pixel clock required by the Video D to A located on the expansion mezzanine board. It also handles memory management for the 512K x 32 SRAM image buffer, and provides the miscellaneous control for the VGA to NTSC/PAL encoder, which are both located on the expansion mezzanine board.

The output of the video generator is fed to a video Digital to Analog Converter (D/A). The image data, or pixel data, is transmitted as three color channels, Red, Green and Blue with each channel supporting 10-bits of resolution. Data sent to the video D/A is synchronous with the sync and blanking control using a pixel clock generated by the VGA IP.

C. Image Pattern Buffer

The Cyclone III FPGA does not have enough internal memory to hold a full color 640 x 480 VGA image, so an external 512K x 32 Static Random Access Memory (SRAM) was added to the expansion mezzanine board. Control of the SRAM is done via a memory management unit integrated within the video IP core. Simply writing the equivalent of a bitmap image to the SRAM will cause the image to be displayed on the selected video output (VGA, NTSC or PAL) - once the instrument is placed in the run state.

D. Video D/A (ADV7123)

The ADV7123 is a triple channel, high speed, digital-to-analog converter marketed by Analog Devices. It consists of three high-speed, 10-bit, video D/A converters (channels) with complementary outputs and a standard TTL input interface [4]. The ADV7123 is compatible with a wide variety of high-resolution color graphics systems including, NTSC (RS-170A).

RGB data, synchronization and blanking control from the VGA IP core interface to the ADV7123 and are synchronous with the pixel clock, which is also supplied by the IP core. The pixel clock is determined by a simple calculation using the horizontal and vertical resolution of the image (640 x 480), the refresh rate (60 Hz) and the retrace time, or blanking factor (0.8). For a 640 x 480 display, the pixel clock is 23.04 MHz.

E. NTSC / PAL Encoder (AD725)

The output of the ADV7123 video D/A is a VGA signal. To support NTSC and PAL video signals, a VGA-to-Composite encoder is used. The AD725, from Analog Devices, is a very low cost general purpose RGB to NTSC/PAL encoder that converts red, green and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance (subcarrier amplitude and phase) signals in accordance with either the NTSC or PAL standards [5].

In order to support NTSC or PAL video standards, the image data must be presented to the encoder in an interlaced format. Normally, VGA is non-interlaced, so a control in the video IP has been added that, when asserted, causes the video IP core to present the image data to the encoder in an odd/even interlaced format. The encoder requires a clock that is 4x the color subcarrier of the standard selected, 14.318180MHz for NTSC or 17.734475MHz for PAL. These clocks are provided by dedicated crystal oscillators for stability, and are selected via a multiplexer controlled by the FPGA. The pixel clock and other timing parameters of the video D to A are programmed appropriately to accommodate the different resolutions for either the NTSC or PAL formats. Figure 2 shows the PXI FPGA module with the application specific mezzanine card.

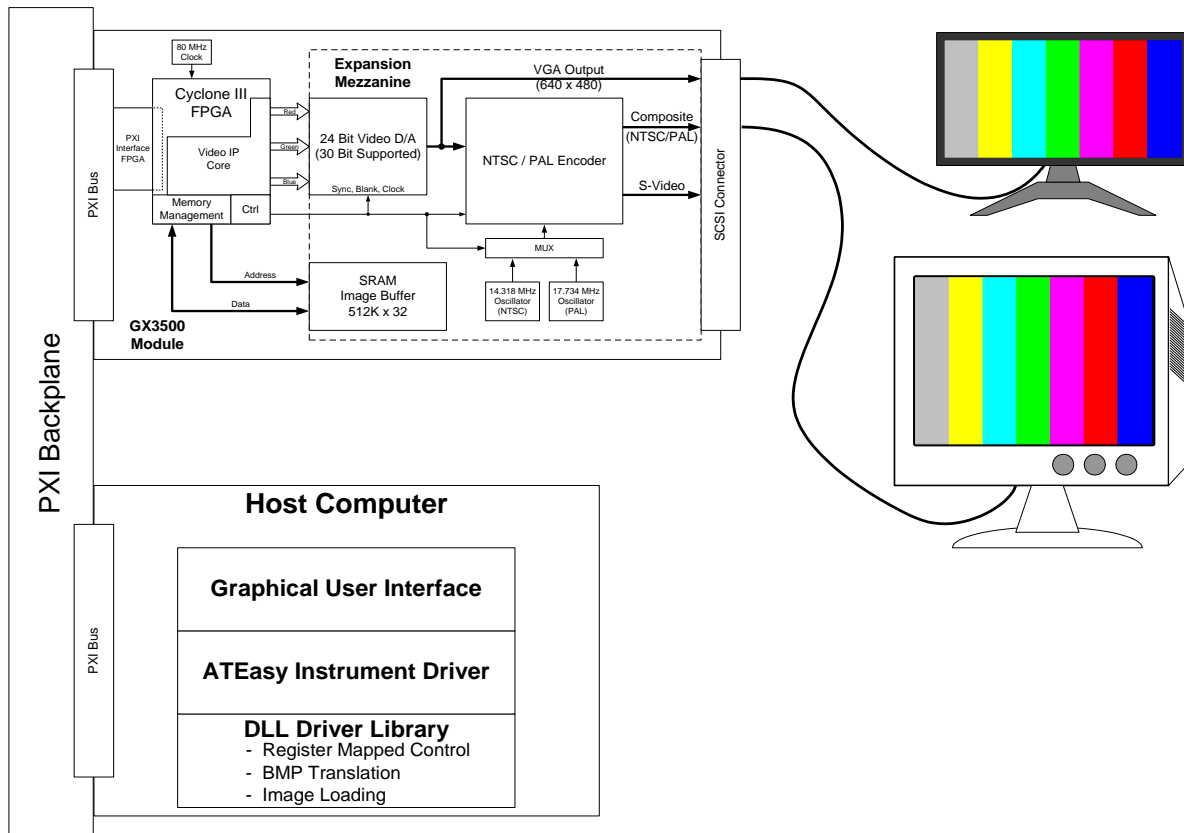Figure 2 - 3U PXI Video Pattern Generator Module

Figure 3 - PXI Video Test Pattern System

III. SOFTWARE

The video generator hardware is controlled by reads and writes to various control registers within the Cyclone III. A low-level driver library provides function calls to load images, select video standards, and enable the hardware to actively display the image stored in the SRAM buffer. The driver library is distributed as a DLL that easily integrates with any Windows-based programming language. A function for loading bitmapped images to the image buffer allows test patterns to be displayed for the selected display type. The function accepts the path and name for the displayed BMP image file and converts the 24-bit BMP image
(8 bits for each color channel) to 30 bits (10 bits for each color channel) by shifting the data left two bit positions to align with the MSB of the 10-bit pattern – effectively padding the two LSB's of each 10-bit color channel. The integrated test system with the video test pattern generator is depicted in Figure 3. High-level control consists of predefined test patterns that can be selected and loaded to the video generator from the host computer. The user has the option to select the destination for the video content, VGA, NTSC or PAL, and the software will set the control registers accordingly.

IV. SUMMARY

Combining a flexible FPGA platform with a handful of commercially available components and control software, offers a flexible and cost effective video test solution for supporting legacy display devices using current technology and the PXI platform. For many display or video processor test needs, using a standard PXI FPGA product with an application specific mezzanine card offers a cost effective and compact video generator solution – eliminating the need for an expensive, stand-alone video generator.

REFERENCES

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[4] Analog Devices ADV7123 Data Sheet

[5] Analog Devices AD725 Data Sheet