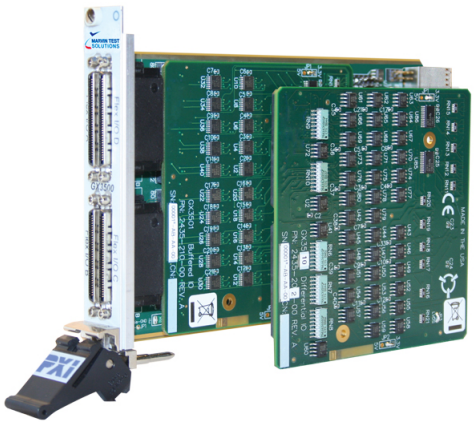
GX3500

MARVIN TEST SOLUTIONS

FPGA PXI DIGITAL I/O CARD

- User configurable, on-board Intel/Altera Cyclone III FPGA device
- Module software is fully compatible with Intel/Altera object files
- No proprietary FPGA design tools required
- Compatible with Intel/Altera's free web-based Quartus II design tools
- 160 digital I/O signals available for application support
- Accommodates standard and custom expansion boards
- Compatible I/O with NI PXI 7811R / 7813R FPGA's
- PXI hybrid slot compatible



DESCRIPTION

The GX3500 is a user configurable 3U FPGA PXI card which offers 160 digital I/O signals for specific application needs, as well as providing pin for pin compatibility with NI PXI 7811R and 7813R FPGA cards. The card employs the Altera Cyclone III FPGA which can support clock rates up to 150 MHz and features over 55,000 logic elements and 2.34 Mb of memory. The 3U PXI FPGA card GX3500 can also accept an expansion card assembly which can be used to customize the interface to the UUT – eliminating the need for additional external boards which are cumbersome and physically difficult to integrate into a test system. The design of the FPGA is done by using Altera's free Quartus II Web Edition tool set. Once the user has compiled the FPGA design, the image can be loaded into the FPGA via the PXI bus interface or via an on-board EEPROM.

FEATURES

The GX3500's four banks of 40 digital I/O signals can be selectively isolated from the I/O connectors under software control. The signals are 5 V tolerant. Logic families supported by the I/O interface include LVTTL and LVCMOS. The FPGA device supports up to four phase lock loops for clock synthesis, clock generation and for support of the I/O interface. An on-board 80 MHz oscillator is available for use with the FGPA device or alternatively, the PXI 10 MHz clock can be used as a clock reference by the FPGA.

The FPGA has access to all of the PXI bus resources including the PXI 10 MHz clock, the local bus, and the PXI triggers, allowing the user to create a custom instrument which incorporates all of the PXIbus' resources. Control and access to the FPGA is provided via the GX3500's driver (GxFPGA) which includes tools for downloading the compiled FPGA code as well as providing register read and write functionality.

The GX3500 can be configured with several different standard expansion boards - providing buffered I/O interfaces for TTL, LVDS, differential TTL and ECL logic families. Additionally, the GX3500 can be configured with a video generator board which supports VGA, PAL ,and NTSC interfaces.

PROGRAMMING AND SOFTWARE

The board is supplied with the GXFPGA library, a software package that includes a virtual instrument panel, and a Windows 32/64-bit DLL driver library and documentation. The virtual panel can be used to interactively program and control the instrument from a window that displays the instrument's current settings and status. In addition, interface files are provided to support access to programming tools and languages such as ATEasy, LabView, LabView/Real-Time, C/C++, Microsoft Visual Basic®, Delphi, and Pascal. An On-Line help file and PDF User's Guide provides documentation that includes instructions for installing, using and programming the board.
A separate software package - GtLinux - provides support for Linux 32/64 operating systems.

APPLICATIONS

- Automatic Test Equipment (ATE)
- Semiconductor test
- Custom interface emulation
- Custom instrumentation

FPGA

GX3500

SPECIFICATIONS

DIGITAL I/O CHANNELS	
Logic Families	LVTTL and LVCMOS, 5 V compatible
Output Current	±4.0 mA
Input Leakage Current	±10 µA
Power on State	Default is disconnect at power on or user programmable via jumpers
Number of Channels	4 banks of 40 I/O signals. Direction is configurable on a per pin basis Disconnect on a per bank basis
Protection	Overvoltage: -0.5 V to 7.0 V (input) Short circuit: up to 8 outputs may be shorted at a time
Connector	(4) SCSI III, VHDCI type, 68 pin female
EXPANSION BOARD INTERFACE	
Board ID	4 bits
Digital I/O	160, each bank of 40 can be configured to bypass or access the expansion board
FPGA Flex I/O	4 signals
Master Clear	From PXI interface
Power	±12 V, +5 V, +3.3 V, +2.5 V, +1.2 V
TIMING SOURCES	
PXI Bus	10 MHz
Internal	80 MHz oscillator, ±20 ppm
PCI Clock	33 MHz
FPGA	
FPGA Type	Altera Cyclone III, EP3C55 F484
Number of PLLs	Four
Logic Elements	55,856
Internal Memory	2.34 Mb
POWER (NO EXPANSION BOARD)	
3.3 VDC	400 mA (typ); 1 A (max)
5 VDC	300 mA (typ); 1.2 A (max)
12 VDC (For Expansion Board)	1 A (max)

ENVIRONMENTAL	
Operating Temperature	0 °C to +50 °C
Storage Temperature	-20 °C to +70 °C
Size	3U PXI
Weight	200 g

Note: Specifications are subject to change without notice

ORDERING INFORMATION

GX3500	Flex DIO FPGA Card
GX3500-M	Flex DIO FPGA Card (Ruggedized and conformal coated)
I/O MODULE	
GX3501	80 Channel TTL Buffer Expansion Board for GX3500
GX3509	80 Channel Differential TTL Expansion Board for GX3500
GX3510	80 Channel mLVDS Buffer Expansion Board for GX3500
GX3540	40 Channel ECL Expansion Board for GX3500
GX3511	80 Channel LVDS Buffer Expansion Board for GX3500
ACCESSORY	
GT95015	Connector Interface for all Gx5xxx/GX3xxx, SCSI to 100 Mil Grid, Differential
GT95021	2 ft. Shielded Cable for all 5xxx/35xx (68 Pin)
GT95022	3 ft Shielded Cable for all 5xxx/35xx (68 Pin)
GT95022E	3 ft Shielded Cable for all 5xxx/35xx (68 Pin) Not Terminated One End
GT95025	Connector Interface, 68-Pin SCSI to TTI Testron 170-Pin Signal Block
GT95028	10 ft shielded cable for 5xxx/35xx products (68 Pin)
GT95031	6 ft Shielded Cable for all 5xxx/35xx (68 Pin)
GT95035E-48	Shielded Flying Lead Cable for all 5xxx/35xx (68 Pin), 48".
GX98303	3U "Wireless" Scout Adapter for GX528x/GX529x/GX564x/GX5733 (200-Pin Connector)
GT95021R	2 ft Shielded Cable for all 5xxx/35xx (68 Pin), reversed back shell on one end